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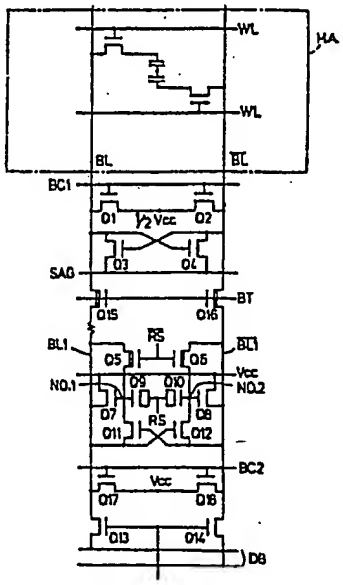
(54) Semiconductor memory device.

(57) A semiconductor memory device comprises a memory cell array (MA), a bit line charge-up circuit (Q1,Q2) coupled to one of a plurality of pairs of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) from the memory cell arry (MA) for initially charging up the one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) to a first voltage which is lower that a power source voltage (Vcc) used to drive the semiconductor memory device, an active restore circuit (Q5-Q12) coupled to the one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) and a switching circuit (Q15,Q16) coupled to the one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) for disconnecting the one pair of bit lines (B1,$\overline{BL}$,BL1,$\overline{BL1}$) into a first pair of bit line sections (BL,BL) on the site of the memory cell array (MA) and a second pair of bit line sections (BL1,$\overline{BL1}$) on the side of the active restore circuit (Q5-Q12) after the one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) are initially charged up to the first voltage. The active restore circuit (Q5-Q12) charges up one of the pair of bit line sections (BL1,$\overline{BL1}$) on the side of the active restore circuit (Q5-Q12) to a second voltage which is higher that the first voltage depending on an datum read out from the memory cell array (MA).

FIG. 3



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AM

TITLE OF THE INVENTION

SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

The present invention generally relates to semiconductor memory devices, and more particularly to a semiconductor memory device such as a dynamic random access memory (DRAM) comprising one-transistor one-capacitor type memory cells, in which it is possible to reduce the power consumption compared to conventional semiconductor memory devices.

An example of a conventional semiconductor memory device generally comprises a memory cell array, a bit line charge-up circuit, a sense amplifier circuit, an active restore circuit and a column select circuit with respect to a pair of bit lines. The pair of bit lines from the memory cell array are coupled to each of the bit line charge-up circuit, the sense amplifier circuit, the active restore circuit and the column select circuit. The bit line charge-up circuit is used to initially charge the bit lines to a power source voltage. A datum (voltage) is read out from a memory cell within the memory cell array by use of the sense amplifier circuit which senses and amplifies the voltage read out via the bit lines. Hence, a small difference in the potentials at the bit lines is amplified and supplied to the active restore circuit. However, there is an inevitable decrease in the potential when the voltage is read out from the memory cell array by use of the sense amplifier circuit, and the active restore circuit is used to compensate for this decrease in the potential by amplification. Out of a plurality of such amplified signals from a plurality of active restore circuits, the column select circuit selectively passes a

signal obtained from one pair of bit lines and supplies this signal to an external data file, for example, via a data bus.

However, a charge-up current or a discharge current in the pair of bit lines can be described by the following equation and is considerably large.

[Charge-up current (or discharge current)]
= [(Potential at bit line) x (Capacitance)]/[Time]

Accordingly, in order to reduce the power consumption, semiconductor memory devices have been recently proposed in which the initial charge-up voltage is made less than or equal to one-half the power source voltage. When the initial charge-up voltage is one-half the power source voltage, the charge-up current becomes one-half that of the conventional semiconductor memory device described before.

But as will be described later on in the specification in conjunction with the drawings, when the initial charge-up voltage is reduced to less than or equal to one-half the power source voltage and the active restore circuit of the conventional semiconductor memory device is used as it is, it is extremely difficult to increase the potentials at the bit lines from this reduced charge-up voltage to the power source voltage. As a result, there are problems in that the power consumption of the semiconductor memory device cannot be reduced considerably without introducing undesirable effects on the operation of the semiconductor memory device.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor memory device in which the problems

described heretofore are eliminated.

Another and more specific object of the present invention is to provide a semiconductor memory device in which bit lines are initially charged up to a first voltage which is lower than a power source voltage and the bit lines are thereafter charged up to a second voltage which is higher than the first voltage. According to the semiconductor memory device of the present invention, the power consumption is reduced because the bit lines are initially only charged up to the first voltage. Furthermore, although the bit lines are initially only charged up to the first voltage, it is possible to positively charge up the bit line to the second voltage depending on a read out datum so that a normal operation of the semiconductor memory device is ensured.

Still another object of the present invention is to provide a semiconductor memory device comprising a memory cell array comprising memory cells, a plurality of pairs of bit lines which are coupled to the memory cells of the memory cell array, a bit line charge-up circuit coupled to one of the plurality of pairs of bit lines for initially charging up the one pair of bit lines from the memory cell array to a first voltage which is lower than a power source voltage used to drive the semiconductor memory device, an active restore circuit coupled to the one pair of bit lines and a switching circuit coupled to the one pair of bit lines for disconnecting the one pair of bit lines into a first pair of bit line sections on the side of the memory cell array and a second pair of bit line sections on the side of the active restore circuit after the one pair of bit lines are initially charged up to the first voltage, wherein the active restore circuit charges up one of the pair of bit line sections on the

side of the active restore circuit to a second voltage which is higher than the first voltage depending on a datum read out from the memory cell array. According to the semiconductor memory device of the present invention, the power consumption of the semiconductor memory device is reduced and the normal operation of the semiconductor memory device is ensured.

A further object of the present invention is to provide a semiconductor memory device which further comprises another bit line charge-up circuit on the side of the active restore circuit for charging up the pair of bit line sections on the side of the active restore circuit to a third voltage which is greater than the first voltage and smaller than the second voltage, wherein the two bit line charge-up circuits are controlled independently by two different signals. According to the semiconductor memory device of the present invention, the charge-up of the bit line from the third voltage to the second voltage depending on the datum read out from the memory cell array can be performed at a high speed so that the semiconductor memory device is unaffected by a voltage fluctuation in the power source voltage.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a circuit diagram showing an essential part of an example of the conventional semiconductor memory device;

FIG.2 is a diagram showing changes in the potentials with respect to time at various parts of the

semiconductor memory device shown in FIG.1;

FIG.3 is a circuit diagram showing an essential part of an embodiment of the semiconductor memory device according to the present invention;

FIGS.4A and 4B are diagrams showing changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.3 for explaining the operation of a first embodiment of the present invention; and

FIGS.5A and 5B are diagrams showing changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.3 for explaining the operation of a second embodiment of the present invention.

DETAILED DESCRIPTION

First, description will be given with respect to the operation of an example of the conventional semiconductor memory device by referring to FIGS.1 and 2. As shown in FIG.1, the conventional semiconductor memory device generally comprises a memory cell array MA, a bit line charge-up circuit comprising transistors Q1 and Q2, a sense amplifier circuit comprising transistors Q3 and Q4, an active restore circuit comprising transistors Q5, Q6, Q7, Q8, $\overline{Q9}$, Q10, Q11 and Q12 and a column select circuit comprising transistors Q13 and Q14. A pair of bit lines BL and $\overline{BL}$ from the memory cell array MA are coupled to each of the bit line charge-up circuit, the sense amplifier circuit, the active restore circuit and the column select circuit. Word lines WL are coupled to the memory cell array MA. A signal line BC is coupled to the bit line charge-up circuit, and a signal line SAG is coupled to the sense amplifier circuit. Signal lines RS

and $\overline{RS}$ are coupled to the active restore circuit. In FIG.1, Vcc denotes a positive power source voltage, NO1 and NO2 respectively denote nodes within the active restore circuit and DB denotes a data bus line.

The conventional semiconductor memory device shown in FIG.1 employs the folded bit lines BL and $\overline{BL}$ in order to read out with a satisfactory sensitivity a small charge stored in a memory capacitor which is within the memory cell array MA and has a small capacitance.

When data are read out from the memory cell array MA by use of the sense amplifier circuit, there is an inevitable decrease in the potential. The active restore circuit is provided to compensate for this decrease in the potential by amplification. The data amplified in the active restore circuit are supplied to the column select circuit which selectively passes a datum related to one pair of bit lines. The data selectively passed by the column select circuit is transmitted through the data bus line DB, amplified and supplied to a data file (not shown).

In the conventional semiconductor memory device shown in FIG.1, the potential at a point P is Vcc and the bit lines BL and $\overline{BL}$ are initially charged up to the voltage Vcc by the bit line charge-up circuit. The datum or voltage read out from the memory cell array MA is obtained through these bit lines BL and $\overline{BL}$ which are charged up, and a small difference in the potentials at the bit lines BL and $\overline{BL}$ is amplified and converted into a signal. However, a charge-up current or a discharge current in the bit lines BL and $\overline{BL}$ is considerably large as may be seen from the following equation.

[Charge-up (or discharge) current]
= [(Potential at bit line) x (Capacitance)]/[Time]

Accordingly, in order to reduce the power consumption of the semiconductor memory device, semiconductor memory devices have been recently proposed in which the charge-up voltage is made less than or equal to one-half the voltage Vcc. When the potential at the point P is Vcc/2 and the charge-up voltage is Vcc/2, the charge-up current becomes one-half that of the conventional semiconductor memory device described before.

However, problems occur when the charge-up voltage is made less than or equal to Vcc/2 and the active restore circuit shown in FIG.1 is used as it is. Such problems will now be described in conjunction with FIG.2. FIG.2 shows changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.1. In FIG.2, the designations used in FIG.1 are used to show the potentials at the various parts of the semiconductor memory device, and Vss denotes a ground voltage.

The potential at the point P is Vcc/2. Before the read-out is made from the memory cell array MA, the potentials at the signal lines BC and $\overline{RS}$ are respectively raised to Vcc. Hence, the transistors Q1 and Q2 of the bit line charge-up circuit are initially turned ON, and the potentials at the bit lines BL and $\overline{BL}$ are respectively reset to Vcc/2. At the same time, the transistors Q7 and Q8 of the active restore circuit are also turned ON, and the potentials at the nodes NO1 and NO2 are respectively reset to Vcc/2.

When the mode changes from a stand-by (or reset) mode to an active mode in which the read-out is made, the potentials at the signal lines BC and $\overline{RS}$ respectively decrease toward the ground voltage Vss, and the bit lines BL and $\overline{BL}$ assume floating states. When the potential at

the word line WL increases, a small difference occurs between the potentials at the bit lines BL and $\overline{BL}$ due to a datum ("0" or "1") read out from the memory cell within the memory cell array MA. A signal corresponding to the read out datum is amplified by decreasing the potential at a common source point of the transistors Q1 and Q2 which constitute the sense amplifier circuit. The potential at only the bit line which becomes low decreases from Vcc/2 to Vss, and at the same time, the potential at one of the nodes NO1 and NO2 decreases to Vss. In the case shown in FIG.2, the potential at the bit line $\overline{BL}$ decreases. Hence, the transistor Q12 within the active restore circuit is turned ON and the potential at the node NO2 decreases to Vss. However, the potential at the node NO1 is maintained to Vcc/2.

In this state, the potential at the signal line RS is increased so as to increase the potential at the node NO1 from Vcc/2 by the operation of the transistors Q9 and Q10. In actual practice, metal oxide semiconductor (MOS) diodes are used for the transistors Q9 and Q10.

Normally, the potential at the bit line must be zero when the datum is "0" and Vcc when the datum is "1". Hence, when the datum is "1", the bit line BL must be charged up from Vcc/2 to Vcc. In order to charge up the bit line BL from Vcc/2 to Vcc, it is necessary to increase the potential at the node NO1 and turn the transistor Q7 ON. In this case, it is necessary to increase the potential at the node NO1 to Vcc + Vr, where Vr denotes the threshold voltage of the transistor Q7. The potential at the line RS increases from Vss to Vcc, but the original potential at the node NO1 is Vcc/2. Accordingly, the potential at the node NO1 cannot be increased to Vcc + Vr with ease.

Generally, the capacitance added at the node NO1 must be small compared to the capacitance of the transistor Q9 which is actually a MOS diode. If the capacitance added at the node NO1 were large compared to the capacitance of the transistor Q9, the potential at the node NO1 will not reach a sufficiently large value even when the potential at the node NO1 is increased by the operation of the transistor Q9. Hence, in order to increase the potential at the node NO1 to the sufficiently large value, the capacitance and thus the size of the transistor Q9 (that is, the MOS diode) must be increased. However, since a plurality of active restore circuits are provided in accordance with the interval with which a plurality of pairs of bit lines are provided, it is impossible to relatively reduce the capacitance added at the node NO1 compared to the capacitance of the transistor Q9 by adding a large capacitance. Furthermore, when the large capacitance is added, the load becomes excessively large and a large voltage will be required to increase the potential at the node NO1.

For these reasons, it is extremely difficult to increase the potential at the node NO1 (or NO2) to over Vcc + V_T and charge up the bit line BL (or $\overline{BL}$) to Vcc.

Accordingly, the semiconductor memory device of the present invention is designed so that the bit lines are initially charged up to a first voltage which is lower than Vcc but it is possible to thereafter charge up the bit line to a second voltage which is higher than the first voltage depending on the read out datum, thereby making it possible to reduce the power consumption of the semiconductor memory device without introducing undesirable effects on the operation of the semiconductor memory device.

FIG.3 is a circuit diagram showing an essential part of an embodiment of the semiconductor memory device according to the present invention. In FIG.3, those parts which are the same as those corresponding parts in FIG.1 are designated by the same reference numerals, and description thereof will be omitted. The semiconductor memory device shown in FIG.3 differs from the semiconductor memory device shown in FIG.1 in that a switching circuit comprising transfer gate transistors Q15 and Q16 and a bit line charge-up circuit (hereinafter referred to as a second bit line charge-up circuit) comprising transistors Q17 and Q18 are additionally provided. The switching circuit is provided between the sense amplifier circuit comprising the transistors Q3 and Q4 and the active restore circuit comprising the transistors Q5 through Q12. The switching circuit separates the pair of bit lines into bit line sections BL and $\overline{BL}$ on the side of the memory cell array MA and bit line sections BL1 and $\overline{BL1}$ on the side of the active restore circuit. The second bit line charge-up circuit is used to charge up the bit line sections BL1 and $\overline{BL1}$ to Vcc - Vr. A signal line BC1 is coupled to the bit line charge-up circuit (hereinafter referred to as a first bit line charge-up circuit) comprising the transistors Q1 and Q2, and a signal line BC2 is coupled to the second bit line charge-up circuit. A signal line BT is coupled to the switching circuit.

Description will now be given with respect to a first embodiment of the present invention by referring to FIGS.3, 4A and 4B. FIGS.4A and 4B show changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.3 for explaining the operation of the first embodiment of the present

invention. In FIGS.4A and 4B, the designations used in FIG.3 are used to show the potentials at the various parts of the semiconductor memory device, and Vss denotes the ground voltage. FIG.4A shows the changes in the potentials at circuit parts on the side of the memory cell array MA, and FIG.4A shows the changes in the potentials at circuit parts on the side of the active restore circuit.

In the stand-by mode of the first embodiment, the potentials at the signal lines BC1 and BC2 are respectively increased to Vcc, the bit line sections BL and $\overline{BL}$ are respectively charged up to Vcc/2 and the bit line sections BL1 and $\overline{BL1}$ are respectively charged up to Vcc - Vr. At the same time, the nodes NO1 and NO2 are charged up to Vcc - Vr because the potential at the line $\overline{RS}$ is Vcc. The fact that the potentials at the nodes NO1 and NO2 are Vcc - Vr and high leads to the advantages which will be described later. The transfer gate transistors Q15 and Q16 are turned OFF after the pair of bit lines, that is, the bit line sections BL, $\overline{BL}$, BL1 and $\overline{BL1}$ are initially charged up to Vcc/2. The bit line sections BL, $\overline{BL}$, BL1 and $\overline{BL1}$ assume floating states when the potential at the signal line BC1 is decreased from Vcc.

When the potential at the word line WL is increased, a datum read out from the memory cell within the memory cell array MA is obtained at the bit line sections BL and $\overline{BL}$. The potential at the bit line which is low decreases to Vss when the transistors Q3 and Q4 constituting the sense amplifier circuit are turned ON. When the potential at the signal line $\overline{RS}$ is decreased and the potential at the signal line BT is increased, the bit line sections BL and BL1 become connected and the bit line

sections $\overline{BL}$ and $\overline{BL1}$ become connected.

In the first embodiment, when the potential at the signal line BT is increased after the sense amplifier circuit operates, the potential at the bit line section $\overline{BL}$ decreases to Vss. For this reason, the potential at the node NO2 is also Vss. On the other hand, the potential at the node NO1 is maintained to Vcc - Vr. Accordingly, when the potential at the signal line RS is increased from Vss to Vcc, the potential at the node NO1 becomes higher than than Vcc + Vr and it is thus possible to charge up the bit line sections BL and BL1 to Vcc via the transistor Q7.

The potential Vcc - Vr obtainable at the node NO1 is considerably high compared to the potential Vcc/2 obtainable in the conventional semiconductor memory device shown in FIG.1. Due to this high potential at the node NO1, it is possible to charge up the bit line which is high at a high speed when the potential at the signal line RS is increased from Vss to Vcc.

According to the first embodiment, the semiconductor memory device is initially charged up to a first voltage which is lower than the power source voltage. Hence, the required charge-up current is small and the power consumption can be reduced effectively. Furthermore, after the semiconductor memory device is initially charged up, only the bit lines are charged up to a second voltage which is much higher than the first voltage so that the semiconductor memory device can operate normally. The bit line is charged up to the second voltage from a third voltage which is greater than the first voltage and is smaller than the second voltage, so that it is possible to positively charge up the bit line to the second voltage. For example, the first voltage is less than or equal to Vcc/2, the second voltage

is equal to Vcc and the third voltage is equal to Vcc - Vr.

In the first embodiment described heretofore, the same signal is applied to the signal lines BC1 and BC2 which respectively control the first and second bit line charge-up circuits. However, different signals may be applied to the signal lines BC1 and BC2 so as to independently control the first and second bit line charge-up circuits.

Next, description will be given with respect to a second embodiment of the present invention in which different signals are applied to the signal lines BC1 and BC2, by referring to FIGS.3, 5A and 5B. FIGS.5A and 5B show changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.3 for explaining the operation of the second embodiment of the present invention. In FIGS.5A and 5B, the designations used in FIGS.4A and 4B are also used to show the potentials at the various parts of the semiconductor memory device. FIG.5A shows the changes in the potentials at circuit parts on the side of the memory cell array MA, and FIG.5B shows the changes in the potentials at circuit parts on the side of the active restore circuit.

In the second embodiment, the operation on the side of the memory cell array MA is essentially the same as that of the first embodiment, as may be seen by comparing FIGS.4A and 5A. However, on the side of the active restore circuit in the second embodiment, the potentials at the signal lines BT and $\overline{RS}$ are respectively increased to Vcc in the stand-by mode. Accordingly, the bit line sections BL, $\overline{BL}$, BL1 and $\overline{BL1}$ and the nodes NO1 and NO2 are respectively charged up to Vcc/2, and the

semiconductor memory device is in a perfect stand-by mode.

When the mode of the semiconductor memory device changes to the active mode, the potential at the signal line BC1 decreases and the potential at the word line WL increases to obtain the datum via the bit lines. The read out datum is sensed and amplified in the sense amplifier circuit as in the first embodiment described before. At the same time, however, the potential at the signal line BT is decreased in the second embodiment and the potential at the signal line BC2 is increased while the read out datum is amplified in the sense amplifier circuit. Hence, the second embodiment differs from the first embodiment in that the potentials at the bit line sections BL1 and $\overline{BL1}$ and the nodes NO1 and NO2 are respectively increased from Vcc/2 to Vcc - Vr by decreasing the potential at the signal line BT and increasing the potential at the signal line BC2 while the read out datum is amplified in the sense amplifier circuit.

The rest of the operation of the second embodiment is basically the same as that of the first embodiment. That is, the potentials at the signal line $\overline{RS}$ and the signal line BC1 are respectively decreased, and the potential at the signal line BT is increased. As a result, the potential at the node NO2 becomes Vss and the potential at the node NO1 becomes Vcc - Vr. When the potential at the signal line RS is increased from Vss to Vcc, the potential at the node NO1 becomes over Vcc + Vr and the bit line sections BL and BL1 are respectively charged up to Vcc.

According to the second embodiment, it is possible to obtain effects which are the same as those obtainable in the first embodiment. Furthermore, the charge-up of the bit line to the power source voltage

depending on the read out datum can be performed at a high speed according to the second embodiment.

The second embodiment is advantageous in that the semiconductor memory device is less affected by a voltage fluctuation in the power source voltage compared to the first embodiment. In other words, in the first embodiment described before, the potentials at the signal lines BC1 and BC2 fluctuate when there is a voltage fluctuation in the power source voltage.

Generally, the tolerance of the voltage fluctuation in the power source voltage is in the order of 5 (volts) ± 10 (%) in the case of the semiconductor memory device. When it is assumed that the power source voltage changes from 5.5 (volts) to 4.5 (volts), a similar change occurs in the potentials at the signal lines BC1 and BC2. On the other hand, the potentials at the nodes NO1 and NO2 and the bit line sections BL1 and $\overline{BL1}$ are respectively maintained to the charged up potentials of 5.5 (volts) - Vr. For this reason, after the fluctuation in the power source voltage occurs, the charged up potentials are in excess for the semiconductor memory device to operate at 4.5 (volts), and this excess charge may cause an erroneous operation of the semiconductor memory device of the first embodiment.

However, in the second embodiment, the charge-up time required to charge up the bit line sections BL1 and $\overline{BL1}$ and the nodes NO1 and NO2 to the potential Vcc - Vr by increasing the potential at the signal line BC2 to the power source voltage Vcc is extremely short as may be seen from FIG.5B. The probability that the power source voltage fluctuates within this extremely short charge-up time is extremely small. Hence, the operation of the second embodiment is reliable even if the fluctuation in

the power source voltage should occur.

Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

CLAIMS

1. A semiconductor memory device comprising:
a memory cell array (MA) comprising memory cells;
a plurality of pairs of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) which are coupled to the memory cells of said memory cell array (MA);
a bit line charge-up circuit (Q1,Q2) coupled to one of the plurality of pairs of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) for initially charging up said one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) from said memory cell array (MA) to a first voltage, said first voltage being lower than a power source voltage Vcc used to drive the semiconductor memory device;
an active restore circuit (Q5-Q12) coupled to said one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$);
characterized in
a switching circuit (Q15,Q16) coupled to said one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) for disconnecting said one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) into a first pair of bit line sections (BL,$\overline{BL}$) on the side of said memory cell array (MA) and a second pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) after said one pair of bit lines (BL,$\overline{BL}$,BL1,$\overline{BL1}$) are initially charged up to said first voltage,
said active restore circuit (Q5-Q12) charging up one of the pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) to a second voltage which is higher that said first voltage depending on a datum read out from said memory cell array (MA).

2. A semiconductor memory device as claimed in claim 1, characterized in that said first voltage is less

than or equal to Vcc/2.

3. A semiconductor memory device as claimed in claim 1 or 2, characterized in that said second voltage is equal to Vcc.

4. A semiconductor memory device as claimed in any one of claims 1 to 3, characterized in further comprising a second bit line charge-up circuit (Q17,Q18) coupled to the pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12), said second bit line charge-up circuit (Q17,Q18) charging up said one of the pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) to a third voltage which is higher than said first voltage and is lower than said second voltage.

5. A semiconductor memory device as claimed in claim 4, characterized in that said active restore circuit (Q5-Q12) charges up said one of the pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) from said third voltage to said second voltage depending on the datum read out from said memory cell array (MA).

6. A semiconductor memory device as claimed in claim 4 or 5, characterized in that said active restore circuit comprises a plurality of transistors (Q5-Q12), and said third voltage is selected to Vcc - Vr, where Vr denotes a threshold voltage of one of the transistors constituting said active restore circuit.

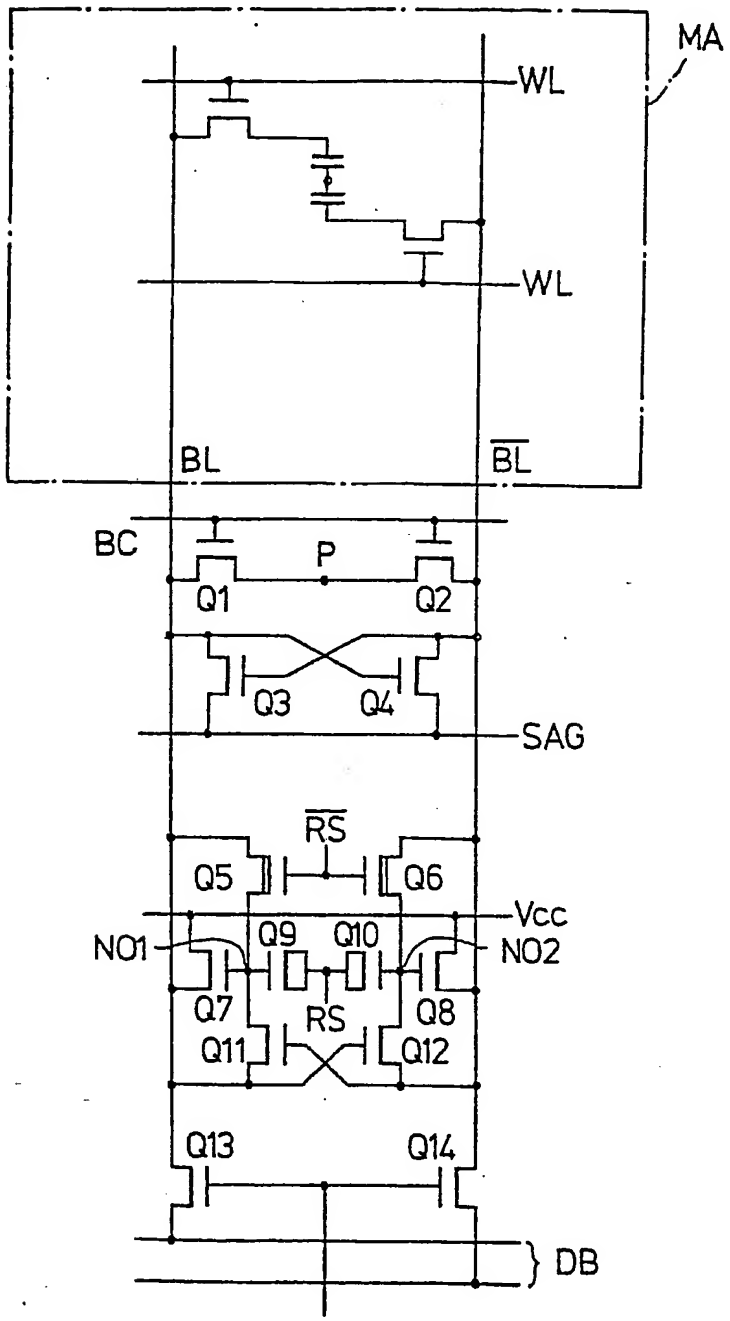
7. A semiconductor memory device as claimed in anyone of claims 4 to 6, characterized in that the two bit line charge-up circuits (Q1,Q2;Q17,Q18) are controlled by the same signal.

8. A semiconductor memory device as claimed in anyone of claims 4 to 6, characterized in that the two bit line charge-up circuits (Q1,Q2;Q17,Q18) are independently controlled by two different signals.

9. A semiconductor memory device as claimed in anyone of claims 1 to 8, characterized in that said pair of bit line sections (BL,$\overline{BL}$) on the side of said memory cell array (MA) and said pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) are respectively charged up to said first voltage in a stand-by mode of said semiconductor memory device.

10. A semiconductor memory device as claimed in anyone of claims 1-8, characterized in that said pair of bit line sections (BL,$\overline{BL}$) on the side of said memory cell array (MA) are charged up to said first voltage and said pair of bit line sections (BL1,$\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) are charged up to a third voltage in a stand-by mode of said semiconductor memory device (MA), said third voltage being higher than said first voltage and smaller than said second voltage.

FIG. 1 PRIOR ART



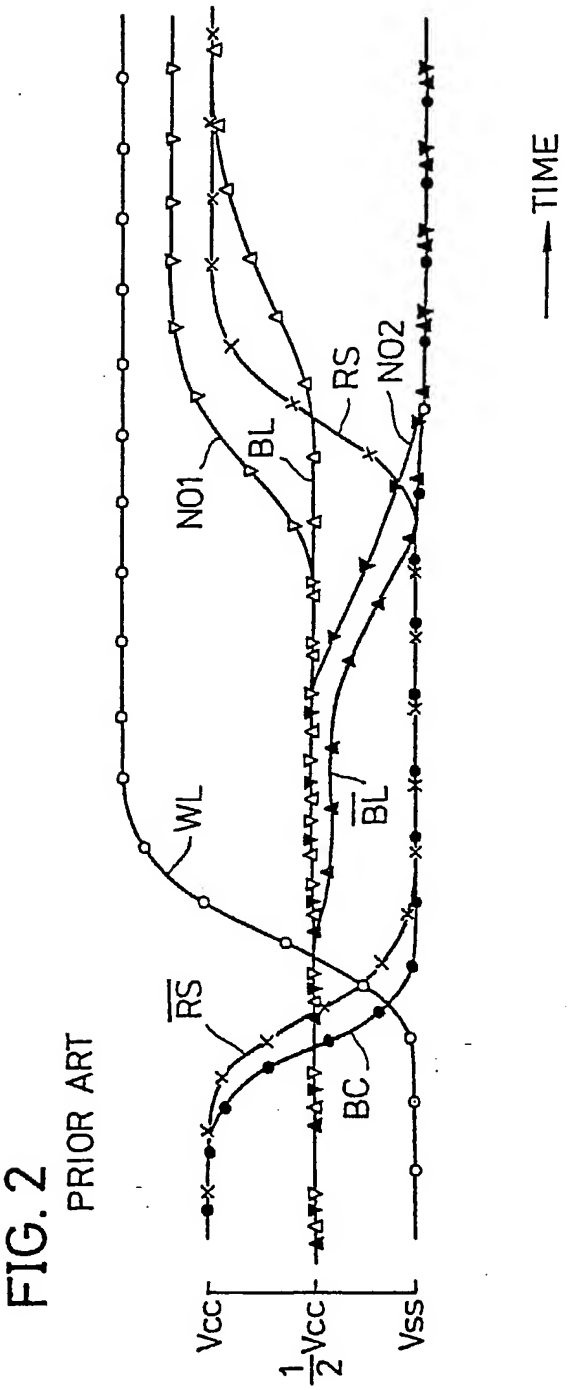


FIG. 2
PRIOR ART

FIG. 3

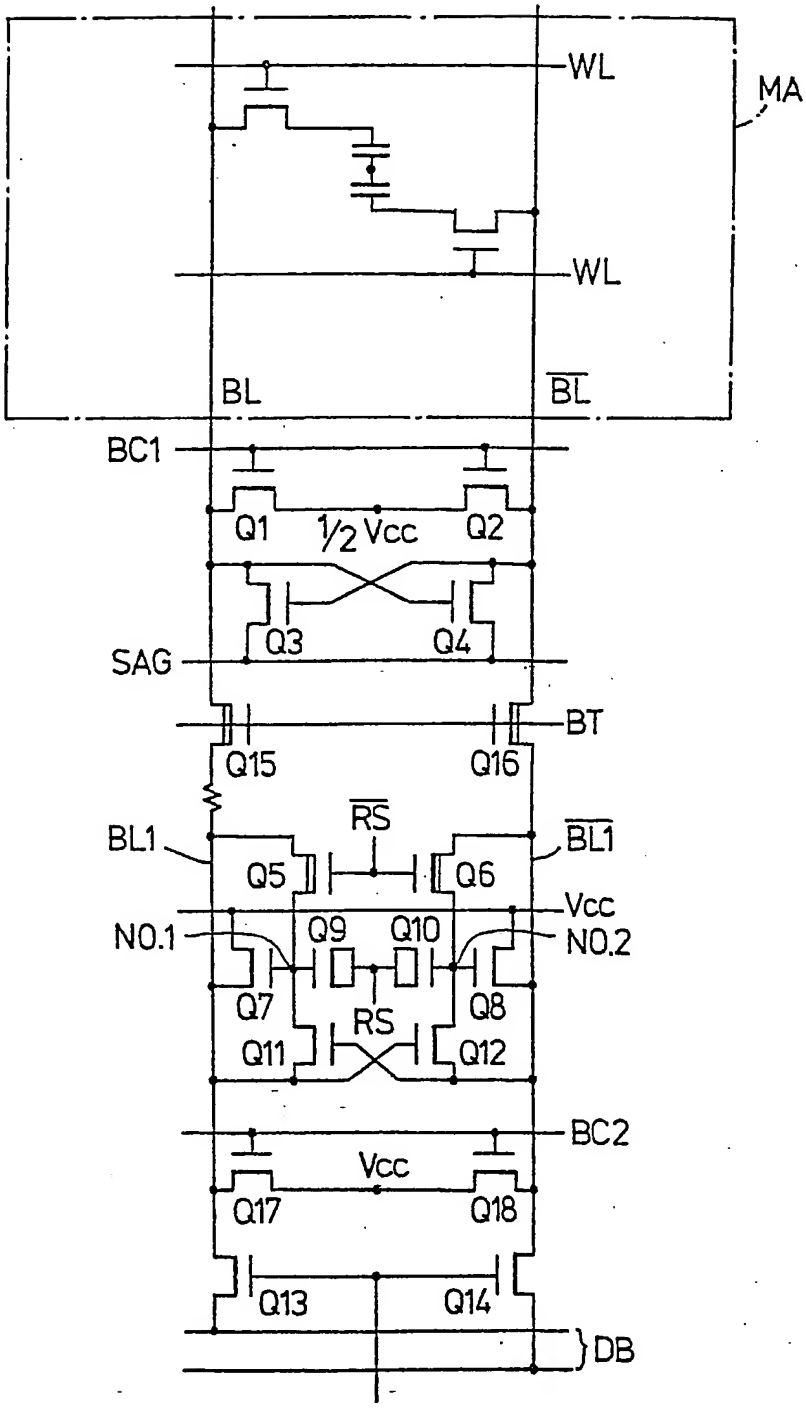

WL
MA
WL
BL
$\overline{BL}$
BC1
Q1
1/2 Vcc
Q2
Q3
Q4
SAG
BT
Q15
Q16
$\overline{RS}$
BL1
$\overline{BL1}$
Q5
Q6
Vcc
NO.1
Q9
Q10
NO.2
Q7
Q8
RS
Q11
Q12
BC2
Vcc
Q17
Q18
Q13
Q14
DB

FIG. 4A

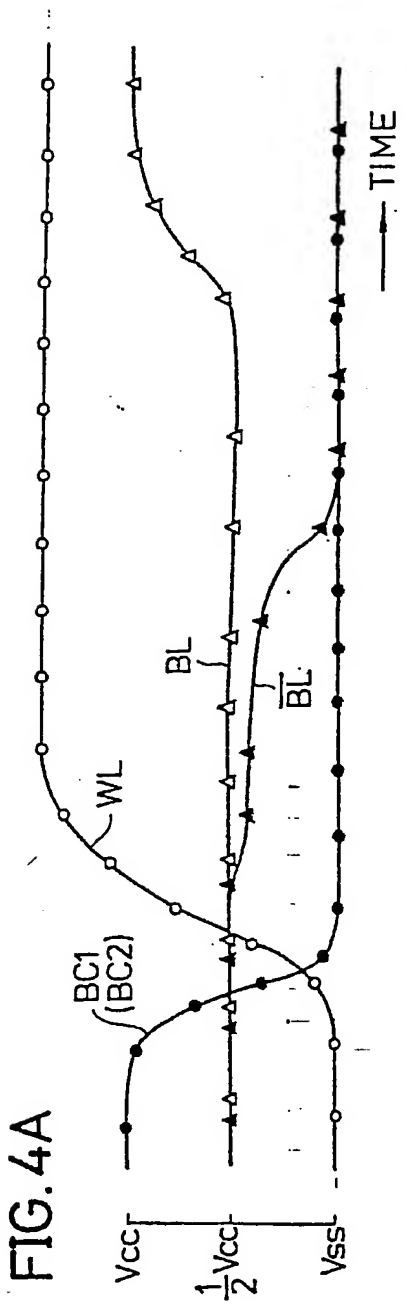

WL
BC1
(BC2)
BL
$\overline{BL}$
Vcc
$\frac{1}{2}$Vcc
Vss
TIME

FIG. 4B

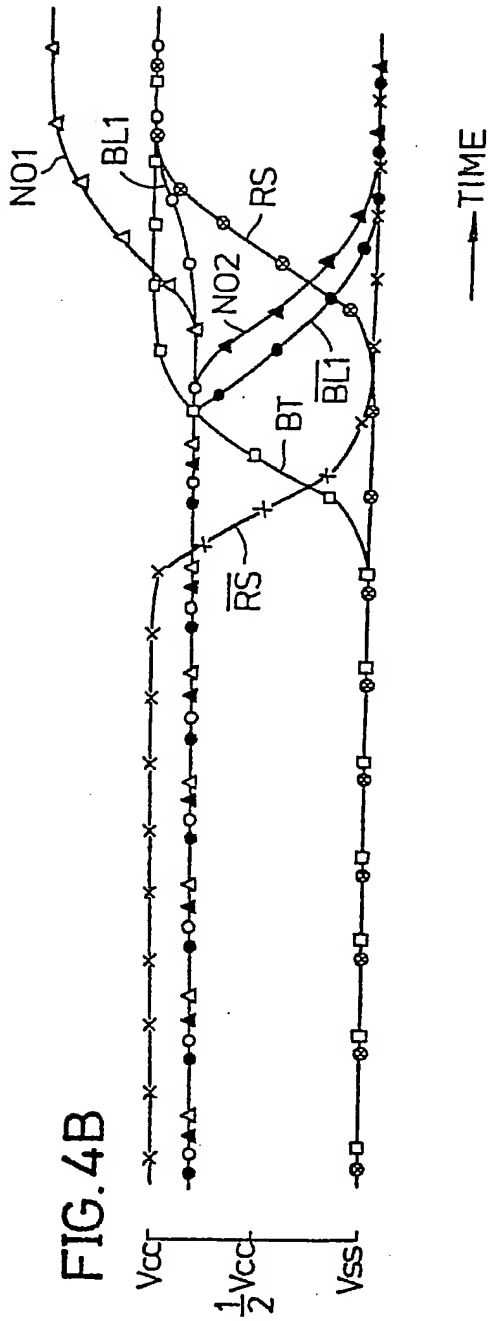

NO1
BL1
RS
NO2
$\overline{BL1}$
BT
$\overline{RS}$
Vcc
$\frac{1}{2}$Vcc
Vss
TIME

FIG. 5A

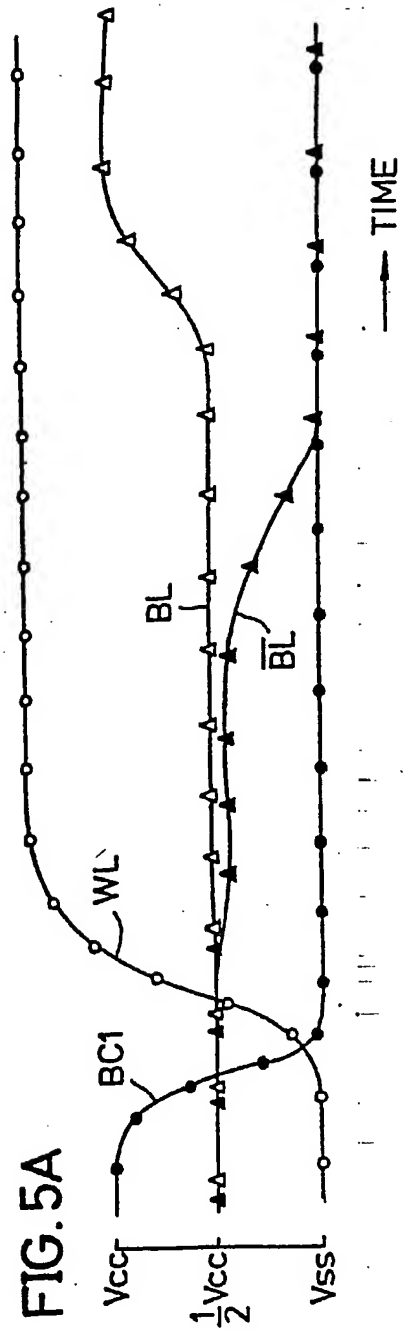
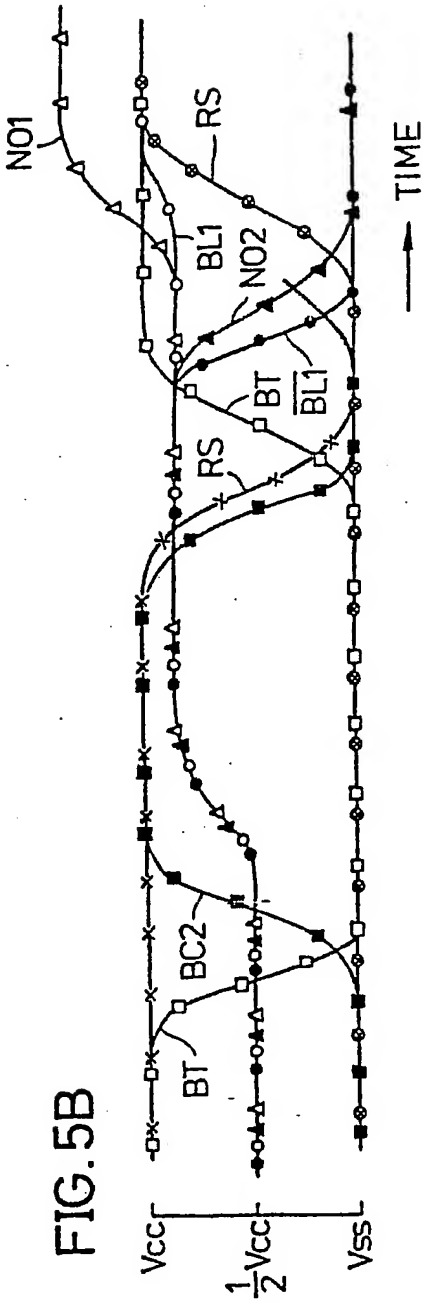

Vcc
1/2Vcc
Vss
WL
BC1
BL
$\overline{BL}$
TIME

FIG. 5B


Vcc
1/2Vcc
Vss
NO1
BC2
BT
RS
BL1
NO2
$\overline{BL1}$
TIME

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US-A- 4 162 416
US-A- 4 247 917

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EP 0 197 505 B1

Description

The present invention generally relates to semiconductor memory devices and it's mode of operation, more particularly to a dynamic random access memory device (DRAM) comprising one-transistor one-capacitor type memory cells, in which device it is possible to reduce the power consumption.

An example of a conventional semiconductor memory device generally comprises a memory cell array, a bit line charge-up circuit, a sense amplifier circuit, an active restore circuit and a column select circuit with respect to a pair of bit lines. The pair of bit lines from the memory cell array are coupled to each of the bit line charge-up circuit, the sense amplifier circuit, the active restore circuit and the column select circuit. The bit line charge-up circuit is used to initially charge the bit lines to a power source voltage. A datum (voltage) is read out from a memory cell within the memory cell array by use of the sense amplifier circuit which senses and amplifies the voltage read out via the bit lines. Hence, a small difference in the potentials at the bit lines is amplified and supplied to the active restore circuit. However, there is an inevitable decrease in the potential when the voltage is read out from the memory cell array by use of the sense amplifier circuit, and the active restore circuit is used to compensate for this decrease in the potential by amplification. Out of a plurality of such amplified signals from a plurality of active restore circuits, the column select circuit selectively passes a signal obtained from one pair of bit lines and supplies this signal to an external data file, for example, via a data bus.

However, a charge-up current or a discharge current in the pair of bit lines can be described by the following equation and is considerably large.

[Charge-up current (or discharge current)]
= [(Potential at bit line) x (Capacitance)]/[Time]

Accordingly, in order to reduce the power consumption, semiconductor memory devices have been recently proposed in which the initial charge-up voltage is made less than or equal to one-half the power source voltage. When the initial charge-up voltage is one-half the power source voltage, the charge-up current becomes one-half that of the conventional semiconductor memory device described before.

In "Electronics and Comm. in Japan", Vol. 65, No. 3 (March 1982), Silver Spring, USA, pages 85-92, a dynamic MOS-RAM with a 1/2 V_{cc}-midpoint bit line precharge is described; the active restore circuit is precharged to V_{cc}. Especially in page 90, Fig. 13 and 14, a memory circuit is disclosed in which a disconnection of the bit lines performed by a signal controled switch, is provided.

There the sense-amplifier or -latch with its cross coupled transistors becomes disconnected from the bit lines as well as from the memory circuit with its midpoint and its active restore circuit. The bit lines and the memory circuit remain connected with their memory cell.

But as will be described later on in the specification in conjunction with the drawings, when the initial charge-up voltage is reduced to less than or equal to one-half the power source voltage and the active restore circuit of the conventional semiconductor memory device is used as it is, it is extremely difficult without fluctuations to increase the potentials at the bit lines from this reduced charge-up voltage to a higher value. According to prior art the power consumption of the semiconductor memory device cannot be reduced considerably without introducing fluctuations on the operation of the semiconductor memory device.

Accordingly, it is object of the present invention to provide a semiconductor memory device operating without fluctuations. The invention is defined in claim 1.

A semiconductor memory device is provided which bit lines are initially charged up to a first voltage which is lower than a power source voltage and the bit lines are thereafter charged up to higher voltages. The power consumption is reduced because the bit lines are initially only charged up to the first voltage. Furthermore, although the bit lines are initially only charged up to the first voltage, it is possible to positively charge up the bit line to a voltage depending on a read out datum so that a normal operation of the semiconductor memory device is ensured.

The semiconductor memory device here used comprises a memory cell array comprising memory cells, a plurality of pairs of bit lines which are coupled to the memory cells of the memory cell array, a first bit line charge-up circuit coupled to one of the plurality of pairs of bit lines for initially charging up the one pair of bit lines from the memory cell array to a first voltage which is lower than a power source voltage used to drive the semiconductor memory device, an active restore circuit coupled to the one pair of bit lines and a switching circuit coupled to the one pair of bit lines for upon a signal disconnecting the one pair of bit lines into a first pair of bit line sections on the side of the memory cell array and a second pair of bit line sections on the side of the active restore circuit after the one pair of bit lines are initially charged up to the first voltage.

The semiconductor memory device comprises a second bit line charge-up circuit on the side of

the active restore circuit for charging up the pair of bit line sections on the side of the active restore circuit to a second voltage which is higher than the first voltage and lower than a third voltage, wherein the two bit line charge-up circuits are controlled independently by two different signals.

After reconnection of the bit line sections the charge-up of the bit line from the second voltage to the third voltage depending on the datum read out from the memory cell array can be performed at a high speed so that the semiconductor memory device is unaffected by a voltage fluctuation in the power source voltage.

Other objects and the features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a circuit diagram showing an essential part of an example of the conventional semiconductor memory device as disclosed in the EP-A-0 114 492, Fig 9;

FIG.2 is a diagram showing changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.1;

FIG.3 is a circuit diagram showing an essential part of an embodiment of the semiconductor memory device used for the present invention;

FIGS.4A and 4B are diagrams showing changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.3 for explaining the operation of the present invention.

DETAILED DESCRIPTION

First, description will be given with respect to the operation of an example of the conventional semiconductor memory device by referring to FIGS.1 and 2. As shown in FIG.1, the conventional semiconductor memory device generally comprises a memory cell array MA, a bit line charge-up circuit comprising transistors Q1 and Q2, a sense amplifier circuit comprising transistors Q3 and Q4, an active restore circuit comprising transistors Q5, Q6, Q7, Q8, Q9, Q10, Q11 and Q12 and a column select circuit comprising transistors Q13 and Q14. A pair of bit lines BL and $\overline{BL}$ from the memory cell array MA are coupled to each of the bit line charge-up circuit, the sense amplifier circuit, the active restore circuit and the column select circuit. Word lines WL are coupled to the memory cell array MA. A signal line BC is coupled to the bit line charge-up circuit, and a signal line SAG is coupled to the sense amplifier circuit. Signal lines RS and $\overline{RS}$ are coupled to the active restore circuit. In FIG.1, Vcc denotes a positive power source voltage, NO1 and NO2 respectively denote nodes within the active restore circuit and DB denotes a data bus line.

The conventional semiconductor memory device shown in FIG.1 employs the folded bit lines BL and $\overline{BL}$ in order to read out with a satisfactory sensitivity a small charge stored in a memory capacitor which is within the memory cell array MA and has a small capacitance.

When data are read out from the memory cell array MA by use of the sense amplifier circuit, there is an inevitable decrease in the potential. The active restore circuit is provided to compensate for this decrease in the potential by amplification. The data amplified in the active restore circuit are supplied to the column select circuit which selectively passes a datum related to one pair of bit lines. The data selectively passed by the column select circuit are transmitted through the data bus line DB, amplified and supplied to a data file (not shown).

In the conventional semiconductor memory device shown in FIG.1, the potential at a point P is Vcc and the bit lines BL and $\overline{BL}$ are initially charged up to the voltage Vcc by the bit line charge-up circuit. The datum or voltage read out from the memory cell array MA is obtained through these bit lines BL and $\overline{BL}$ which are charged up, and a small difference in the potentials at the bit lines BL and $\overline{BL}$ is amplified and converted into a signal. However, a charge-up current or a discharge current in the bit lines BL and $\overline{BL}$ is considerably large as may be seen from the following equation.

[Charge-up (or discharge) current]
= [(Potential at bit line) x (Capacitance)]/[Time]

Accordingly, in order to reduce the power consumption of the semiconductor memory device,the above cited semiconductor memory device has been proposed in which the charge-up voltage is made equal to one-half the voltage Vcc. When the potential at the point P is Vcc/2 and the charge-up voltage is Vcc/2, the charge-up current becomes one-half that of former conventional semiconductor memory devices.

However, problems occur when the charge-up voltage is made less than or equal to Vcc/2 and the active restore circuit shown in FIG.1 is used as it is. Such problems will now be described in conjunction with FIG.2. FIG.2 shows changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.1. In FIG.2, the designations used in FIG.1 are used to show the potentials at the various parts of the

semiconductor memory device, and Vss denotes a ground voltage.

The potential at the point P is Vcc/2. Before the read-out is made from the memory cell array MA, the potentials at the signal lines BC and $\overline{RS}$ are respectively raised to Vcc. Hence, the transistors Q1 and Q2 of the bit line charge-up circuit are initially turned ON, and the potentials at the bit lines BL and $\overline{BL}$ are respectively reset to Vcc/2. At the same time, the transistors Q7 and Q8 of the active restore circuit are also turned ON, and the potentials at the nodes NO1 and NO2 are respectively reset to Vcc/2.

When the mode changes from a stand-by (or reset) mode to an active mode in which the read-out is made, the potentials at the signal lines BC and $\overline{RS}$ respectively decrease toward the ground voltage Vss, and the bit lines BL and $\overline{BL}$ assume floating states. When the potential at the word line WL increases, a small difference occurs between the potentials at the bit lines BL and $\overline{BL}$ due to a datum ("0" or "1") read out from the memory cell within the memory cell array MA. A signal corresponding to the read out datum is amplified by decreasing the potential at a common source point of the transistors Q3 and Q4 which constitute the sense amplifier circuit. The potential at only the bit line which becomes low decreases from Vcc/2 to Vss, and at the same time, the potential at one of the nodes NO1 and NO2 decreases to Vss. In the case shown in FIG.2, the potential at the bit line $\overline{BL}$ decreases. Hence, the transistor Q12 within the active restore circuit is turned ON and the potential at the node NO2 decreases to Vss. However, the potential at the node NO1 is maintained to Vcc/2.

In this state, the potential at the signal line RS is increased so as to increase the potential at the node NO1 from Vcc/2 by the operation of the transistors Q9 and Q10. In actual practice, metal oxide semiconductor (MOS) diodes are used for the transistors Q9 and Q10.

Normally, the potential at the bit line must be zero when the datum is "0" and Vcc when the datum is "1". Hence, when the datum is "1", the bit line BL must be charged up from Vcc/2 to Vcc. In order to charge up the bit line BL from Vcc/2 to Vcc, it is necessary to increase the potential at the node NO1 and turn the transistor Q7 ON. In this case, it is necessary to increase the potential at the node NO1 to Vcc + Vr, where Vr denotes the threshold voltage of the transistor Q7. The potential at the line RS increases from Vss to Vcc, but the original potential at the node NO1 is Vcc/2. Accordingly, the potential at the node NO1 cannot be increased to Vcc + Vr with ease.

Generally, the capacitance added at the node NO1 must be small compared to the capacitance of the transistor Q9 which is actually a MOS diode. If the capacitance added at the node NO1 were large compared to the capacitance of the transistor Q9, the potential at the node NO1 will not reach a sufficiently large value even when the potential at the node NO1 is increased by the operation of the transistor Q9. Hence, in order to increase the potential at the node NO1 to the sufficiently large value, the capacitance and thus the size of the transistor Q9 (that is, the MOS diode) must be increased. However, since a plurality of active restore circuits are provided in accordance with the interval with which a plurality of pairs of bit lines are provided, it is impossible to relatively reduce the capacitance added at the node NO1 compared to the capacitance of the transistor Q9 by adding a large capacitance. Furthermore, when the large capacitance is added, the load becomes excessively large and a large voltage will be required to increase the potential at the node NO1.

For these reasons, it is found extremely difficult to increase the potential at the node NO1 (or NO2) to over Vcc + Vr and charge up the bit line BL (or $\overline{BL}$) to Vcc.

Accordingly, the semiconductor memory device and it's operation according to the present invention is designed so that the bit lines are initially charged up to a first voltage which is lower than Vcc but it is possible to thereafter charge up the bit lines to a second voltage which is higher than the first voltage and then to a third voltage which third voltage depending on the read out datum, thereby making it possible to reduce the power consumption of the semiconductor memory device without introducing undesirable effects on the operation of the semiconductor memory device.

FIG.3 is a circuit diagram showing an essential part of an embodiment of the semiconductor memory device according to the present invention. In FIG.3, those parts which are the same as those corresponding parts in FIG.1 are designated by the same reference numerals, and description thereof will be omitted. The semiconductor memory device shown in FIG.3 differs from the semiconductor memory device shown in FIG.1 in that a switching circuit comprising transfer gate transistors Q15 and Q16 and a bit line charge-up circuit (hereinafter referred to as a second bit line charge-up circuit) comprising transistors Q17 and Q18 are additionally provided. The switching circuit is provided between the sense amplifier circuit comprising the transistors Q3 and Q4 and the active restore circuit comprising the transistors Q5 through Q12. The switching circuit separates the pair of bit lines into bit line sections BL and $\overline{BL}$ on the side of the memory cell array MA and bit line sections BL1 and $\overline{BL1}$ on the side of the active restore circuit. The second bit line charge-up circuit is used to charge up the bit line sections BL1 and $\overline{BL1}$ to Vcc

- Vr. A signal line BC1 is coupled to the bit line charge-up circuit (hereinafter referred to as a first bit line charge-up circuit) comprising the transistors Q1 and Q2, and a signal line BC2 is coupled to the second bit line charge-up circuit. A signal line BT is coupled to the switching circuit.

Description will now be given with respect to the present invention by referring to FIGS.3, 4A and 4B. FIGS.4A and 4B show changes in the potentials with respect to time at various parts of the semiconductor memory device shown in FIG.3 for explaining the operation of the present invention. In FIGS.4A and 4B, the designations used in FIG.3 are used to show the potentials at the various parts of the semiconductor memory device, and Vss denotes the ground voltage. FIG.4A shows the changes in the potentials at circuit parts on the side of the memory cell array MA, and FIG.4B shows the changes in the potentials at circuit parts on the side of the active restore circuit.

In the stand-by mode, different potentials at the signal lines BC1 and BC2 are applied, i.e BC1 is increased to Vcc. The bit line sections BL and $\overline{BL}$ are respectively charged up to Vcc/2 and the bit line sections BL1 and $\overline{BL1}$ are respectively charged up to $Vcc/_2$ r. At the same time, the nodes NO1 and NO2 are charged up to $Vcc/_2$ because the potential at the line $\overline{RS}$ is Vcc. The fact that the potentials at the nodes NO1 and NO2 are Vcc and high leads to the advantages, but which will be described later. The transfer gate transistors Q15 and Q16 are turned OFF after the pair of bit lines, that is, the bit line sections BL, $\overline{BL}$, BL1 and $\overline{BL1}$ are initially charged up to Vcc/2. The bit line sections BL, $\overline{BL}$, assume floating states when the potential at the signal line BC1 is decreased from Vcc.

Later on the potential at the word line WL is increased, a datum read out from the memory cell within the memory cell array MA is obtained at the bit line sections BL and $\overline{BL}$. The potential at the bit line which is low decreases to Vss when the transistors Q3 and Q4 constituting the sense amplifier circuit are turned ON. When the potential at the signal line $\overline{RS}$ is decreased and the potential at the signal line BT is increased, the bit line sections BL and BL1 become connected with each other and the bit line sections $\overline{BL}$ and $\overline{BL1}$ become connected with each other.

When the potential at the signal line BT is increased after the sense amplifier circuit operates, the potential at the bit line section $\overline{BL}$ decreases to Vss. For this reason, the potential at the node NO2 is also Vss. On the other hand, the potential at the node NO1 remains charged up to Vcc - Vr. Accordingly, when the potential at the signal line RS is increased from Vss to Vcc, the potential at the node NO1 becomes higher than than Vcc + Vr and it is thus possible to charge up the bit line sections BL and BL1 to Vcc via the transistor Q7.

The potential Vcc - Vr obtainable at the node NO1 is considerably high compared to the potential Vcc/2 obtainable in the conventional semiconductor memory device shown in FIG.1. Due to this high potential at the node NO1, it is possible to charge up the bit line which is high at a high speed when the potential at the signal line RS is increased from Vss to Vcc.

The semiconductor memory device is initially charged up to a first voltage which is lower than the power source voltage. Hence, the required charge-up current is small and the power consumption can be reduced effectively. Furthermore, after the semiconductor memory device is initially charged up, only the bit lines are charged up to a third voltage which is much higher than the first voltage so that the semiconductor memory device can operate normally. The bit line is charges up to the third voltage from a second voltage which is higher than the first voltage and is lower than the third voltage, so that it is possible to positively charge up the bit line to the third voltage. For example, the first voltage is less than or equal to Vcc/2, the second voltage is equal to Vcc - Vr and the third voltage is equal to Vcc.

As disclosed different signals are applied to the signal lines BC1 and BC2, by referring to FIGS.3, 4A and 4B. As mentioned FIG.4A shows the changes in the potentials at circuit parts on the side of the memory cell array MA, and FIG.4B shows the changes in the potentials at circuit parts on the side of the active restore circuit.

On the side of the active restore circuit, the potentials at the signal lines BT and $\overline{RS}$ are respectively increased to Vcc in the stand-by mode. Accordingly, the bit line sections BL, $\overline{BL}$, BL1 and $\overline{BL1}$ and the nodes NO1 and NO2 are respectively charged up to Vcc/2, and the semiconductor memory device is in a perfect stand-by mode.

When the mode of the semiconductor memory device changes to the active mode, the potential at the signal line BC1 decreases and the potential at the word line WL increases to obtain the datum via the bit lines. The read out datum is sensed and amplified in the sense amplifier circuit. At the same time, however, the potential at the signal line BT is decreased and the potential at the signal line BC2 is increased while the read out datum is amplified in the sense amplifier circuit. The potentials at the bit line sections BL1 and $\overline{BL1}$ and the nodes NO1 and NO2 are respectively increased from Vcc/2 to Vcc - Vr by decreasing the potential at the signal line BT and increasing the potential at the signal line BC2 while the read out datum is amplified in the sense amplifier circuit.

Now the potentials at the signal line $\overline{RS}$ and

the signal line BC1 are respectively decreased, and the potential at the signal line BT is increased. As a result, the potential at the node NO2 becomes Vss and the potential at the node NO1 becomes Vcc - Vr. When the potential at the signal line RS is increased from Vss to Vcc, the potential at the node NO1 becomes more than Vcc + Vr and the bit line sections BL and BL1 are respectively charged up to Vcc.

According to the invention, it is possible to obtain the charge-up of the bit line to the power source voltage depending on the read out datum at a high speed.

The invention is advantageous in that the semiconductor memory device is less affected by a voltage fluctuation in the power source voltage. In other words, the potentials at the signal lines BC1 and BC2 don't fluctuate although there may be a voltage fluctuation in the power source voltage.

Generally, the tolerance of the voltage fluctuation in the power source voltage is in the order of 5 (volts) ± 10 (%) in the case of the semiconductor memory device. When it is assumed that the power source voltage changes from 5.5 (volts) to 4.5 (volts), a similar change occurs in the potentials at the signal lines BC1 and BC2. On the other hand, the potentials at the nodes NO1 and NO2 and the bit line sections BL1 and $\overline{BL1}$ are respectively maintained to the charged up potentials of 5.5 (volts) - Vr. For this reason, after the fluctuation in the power source voltage occurs, the charged up potentials are in excess for the semiconductor memory device to operate at 4.5 (volts), and without the invention this excess charge may cause an erroneous operation of a semiconductor memory device.

However, according to the invention, the charge-up time required to charge up the bit line sections BL1 and $\overline{BL1}$ and the nodes NO1 and NO2 to the potential Vcc - Vr by increasing the potential at the signal line BC2 to the power source voltage Vcc is extremely short as may be seen from FIG.4B. The probability that the power source voltage fluctuates within this extremely short charge-up time is extremely small. Hence, the operation according to the invention is reliable even if the fluctuation in the power source voltage should occur.

Further, the present invention is not limited to this embodiment, but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A semiconductor memory device comprising:
a memory cell array (MA) comprising memory cells;
a plurality of pairs of bit lines (BL, $\overline{BL}$,BL1, $\overline{BL1}$) which are coupled to the memory cells of said memory cell array (MA);
a first bit line charge-up circuit (Q1, Q2) coupled to one of the plurality of pairs of bit lines (BL, $\overline{BL}$, BL1, $\overline{BL1}$) for, upon a first signal (BC1), initially charging up said one pair of bit lines (BL, $\overline{BL}$, BL1, $\overline{BL1}$) of said memory cell array (MA) to a first voltage (1/2 V_{cc}), said first voltage being lower than a power source voltage (Vcc) used to drive said semiconductor memory device;
an active restore circuit (Q5-Q12) coupled to said one pair of bit lines (BL, $\overline{BL}$, BL1, $\overline{BL1}$), said circuit comprising circuit-nodes (NO1, NO2) initially charged up to said first voltage by said first bit line charge-up circuit, control signal inputs (RS, $\overline{RS}$), and means (Q9, Q10) for boosting the voltages on said circuit nodes;
a switching circuit (Q15, Q16) coupled to said one pair of bit lines (BL, $\overline{BL}$, BL1, $\overline{BL1}$) for, upon a second signal (BT) applied to said switching circuit at the beginning of an access cycle, disconnecting said one pair of bit lines (BL, $\overline{BL}$, BL1, $\overline{BL1}$) into a first pair of bit line sections (BL, $\overline{BL}$) on the side of said memory cell array (MA) and a second pair of bit line sections (BL1, $\overline{BL1}$) on the side of said active restore circuit (Q5-Q12),
a second bit line charge-up circuit (Q17, Q18) coupled to said second pair of bit line sections (BL1, $\overline{BL1}$) for, upon a third signal (BC2) applied to said second bit line charge-up circuit (Q17, Q18), charging up said second pair of bit line sections (BL1, $\overline{BL1}$) on the side of said active restore circuit (Q5-Q12) as well as said circuit nodes (NO1, NO2) to a second voltage which is higher than said first voltage after said first pair of bit line sections has been disconnected from said second pair of bit line sections,
whereupon said first and second pairs of bit line sections (BL, $\overline{BL}$; BL1, $\overline{BL1}$) are reconnected with each other by said switching circuit (Q15, Q16), and said active restore circuit (Q5-Q12), in response to activation of said boosting means, charges up one bit line of said one pair of bit lines (BL, $\overline{BL}$; BL1, $\overline{BL1}$) to a third voltage which is higher than said first and said second voltage, said charging up depending on the datum read out from said memory cell of said memory cell array (MA).

2. A semiconductor memory device as claimed in claim 1, characterized in that said third voltage is equal to Vcc.

3. A semiconductor memory device as claimed in

claim 1, characterized in that said active restore circuit comprises a plurality of transistors (Q5-Q12), and said second voltage is selected to Vcc - Vr, where Vr denotes a threshold voltage of one of the transistors constituting said active restore circuit.

Revendications

1. Dispositif de mémorisation à semiconducteur, comprenant :

une matrice de cellules de mémoire (MA) comprenant des cellules de mémoire ;

une pluralité de paires de lignes de bit (BL, $\overline{BL}$, BL1, $\overline{BL1}$) qui sont couplées aux cellules de mémoire de ladite matrice de cellules de mémoire (MA) ;

un premier circuit de charge de lignes de bit (Q1, Q2) couplé à une paire de la pluralité de paires de lignes de bit (BL, $\overline{BL}$, BL1, $\overline{BL1}$) servant, à l'apparition d'un premier signal (BC1), à initialement charger ladite paire de lignes de bit (BL, $\overline{BL}$, BL1, $\overline{BL1}$) de ladite matrice de cellules de mémoire (MA) jusqu'à un premier potentiel (Vcc/2), ledit premier potentiel étant inférieur à la tension d'une source d'alimentation électrique (Vcc) servant à exciter ledit dispositif de mémorisation à semiconducteur ;

un circuit de restauration active (Q5 à Q12) couplé à ladite paire de lignes de bit (BL, $\overline{BL}$, BL1, $\overline{BL1}$), ledit circuit comprenant des noeuds de circuit (NO1, NO2) initialement chargés jusqu'audit premier potentiel par ledit premier circuit de charge de lignes de bit, des entrées de signaux de commande (RS, $\overline{RS}$), et des moyens (Q9, Q10) servant à élever les tensions présentes sur lesdits noeuds de circuit ;

un circuit de commutation (Q15, Q16) couplé à ladite paire de lignes de bit (BL, $\overline{BL}$, BL1, $\overline{BL1}$) servant, à l'apparition d'un deuxième signal (BT) appliqué audit circuit de commutation au début d'un cycle d'accès, à déconnecter ladite paire de lignes de bit (BL, $\overline{BL}$, BL1, $\overline{BL1}$) en une première paire de sections de ligne de bit (BL, $\overline{BL}$) se trouvant du côté de ladite matrice de cellules de mémoire (MA) et en une deuxième paire de sections de ligne de bit (BL1, $\overline{BL1}$) se trouvant du côté dudit circuit de restauration active (Q5 à Q12) ;

un deuxième circuit de charge de lignes de bit (Q17, Q18) couplé à ladite deuxième paire de sections de ligne de bit (BL1, $\overline{BL1}$) et servant, à l'application d'un troisième signal (BC2) audit deuxième circuit de charge de lignes de bit (Q17, Q18), à charger ladite deuxième section de ligne de bit (BL1, $\overline{BL1}$) se trouvant du côté dudit circuit de restauration active (Q5 à Q12) ainsi que lesdits noeuds de circuit (NO1, NO2) jusqu'à un deuxième potentiel qui est inférieur audit premier potentiel après que ladite première paire de sections de ligne de bit a été déconnectée vis-à-vis de ladite deuxième paire de sections de ligne de bit ;

si bien que lesdites première et deuxième paires de sections de ligne de bit (BL, $\overline{BL}$; BL1, $\overline{BL1}$) sont reconnectées ensemble par ledit circuit de commutation (Q15, Q16) ; et

ledit circuit de restauration active (Q5 à Q12), en réponse à l'activation dudit moyen d'élévation, charge une ligne de bit de ladite paire de lignes (BL, $\overline{BL}$; BL1, $\overline{BL1}$) jusqu'à un troisième potentiel qui est supérieur audit premier et audit deuxième potentiel, ladite opération de charge dépendant de la donnée lue dans ladite cellule de mémoire de ladite matrice de cellules de mémoire (MA).

2. Dispositif de mémorisation à semiconducteur selon la revendication 1, caractérisé en ce que ladite troisième tension est égale à Vcc.

3. Dispositif de mémorisation à semiconducteur selon la revendication 1, caractérisé en ce que ledit circuit de restauration active comprend une pluralité de transistors (Q5 à Q12), et le deuxième potentiel est sélectionné de façon à valoir Vcc - Vr, où Vr désigne la tension de seuil de l'un des transistors constituant ledit circuit de restauration active.

Patentansprüche

1. Halbleiterspeicheranordnung, bestehend aus

einem Speicherzellen-Array (MA) mit Speicherzellen,

einer Mehrzahl von mit den Speicherzellen des Speicherzellen-Arrays (MA) verbundenen Bitleitungspaaren (BL, $\overline{BL}$, BL1, $\overline{BL1}$),

einer mit einem Bitleitungspaar aus der Mehrzahl Bitleitungspaaren (BL, $\overline{BL}$, BL1, $\overline{BL1}$) verbundenen ersten Bitleitungs-Aufladeschaltung (Q1, Q2), die dazu dient, dieses eine Bitleitungspaar (BL, $\overline{BL}$, BL1, $\overline{BL1}$) des Speicherzellen-Arrays (MA) beim Auftreten eines ersten Signals (BC1) anfänglich auf eine erste Spannung (1/2 Vcc) aufzuladen, wobei diese erste Spannung kleiner ist als die für den Betrieb der Halbleiterspeicheranordnung verwendete Versorgungsspannung (Vcc),

einer mit dem einen Bitleitungspaar (BL, $\overline{BL}$, BL1, $\overline{BL1}$) verbundenen aktiven Rückstellschaltung (Q5-Q6) mit Schaltungsknotenpunkten (NO1, NO2), die anfänglich von der ersten

Bitleitungs-Aufladeschaltung auf die genannte erste Spannung aufgeladen werden, ferner mit Steuersignaleingängen (RS, $\overline{RS}$) sowie mit Mitteln (Q9, Q10) zur Erhöhung der Spannungen an den Schaltungsknotenpunkten,

einem mit dem einen Bitleitungspaar (BL, $\overline{BL}$, BL1, $\overline{BL1}$) verbundenen Schalterkreis (Q15, Q16), der dazu dient, beim Anlegen eines zweiten Signals ($\overline{BT}$) an den Schalterkreis zu Beginn eines Zugriffszyklus das eine Bitleitungspaar (BL, $\overline{BL}$, BL1, $\overline{BL1}$) in ein erstes von Bitleitungsabschnitten (BL, BL) auf der Seite des Speicherzellen-Arrays (MA) und ein zweites Paar von Bitleitungsabschnitten (BL1, BL1) auf der Seite der aktiven Rückstellschaltung (Q5-Q12) aufzutrennen,

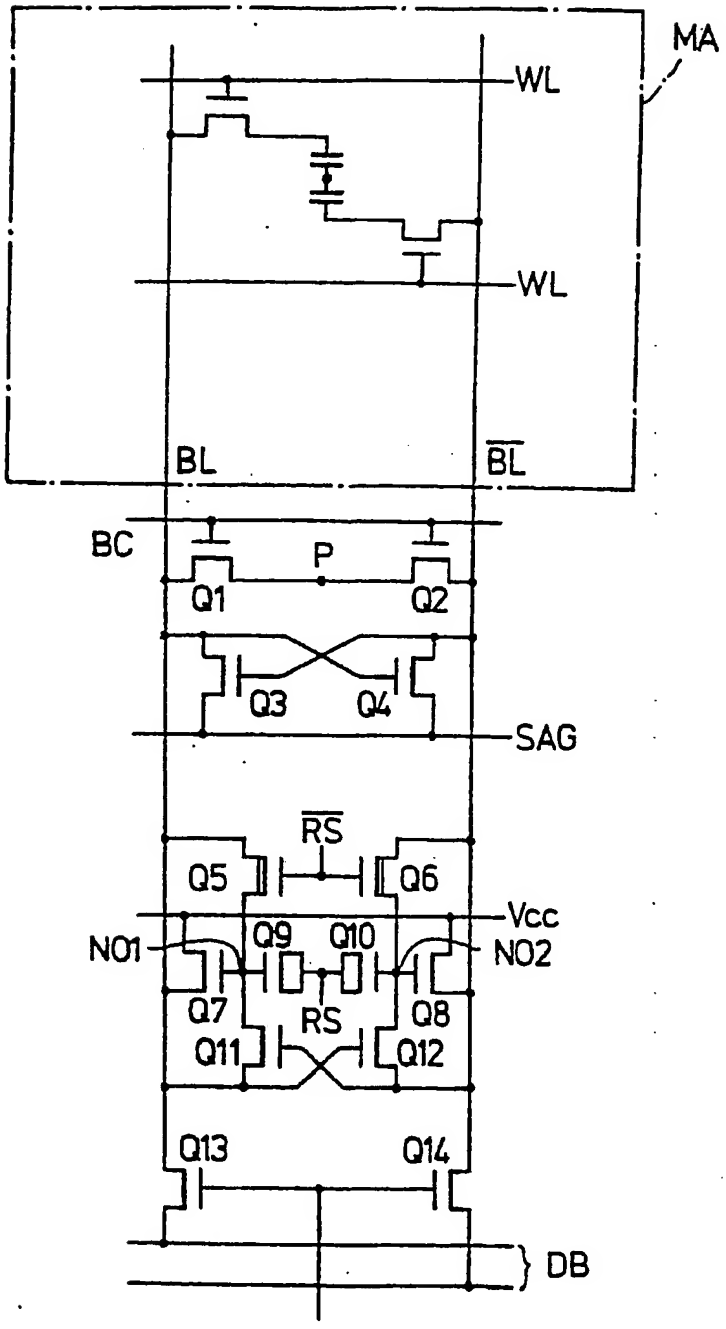
und einer mit dem zweiten Paar von Bitleitungsabschnitten (BL1, $\overline{BL1}$) verbundenen zweiten Bitleitungs-Aufladeschaltung (Q17, Q18), die dazu dient, nach dem Abtrennen des ersten Paares von Bitleitungsabschnitten von dem zweiten Paar von Bitleitungsabschnitten beim Anlegen einer dritten Signal (BC2) an die zweite Bitleitungs-Aufladeschaltung (Q17, Q18) das auf der Seite der aktiven Rückstellschaltung (Q5-Q12) liegende zweite Paar von Bitleitungsabschnitten (BL1, $\overline{BL1}$) und die genannten Schaltungsknotenpunkte (NO1, NO2) auf eine zweite Spannung aufzuladen, die größer ist als die erste Spannung, woraufhin das erste und das zweite Paar von Bitleitungsabschnitten (BL, $\overline{BL}$; BL1, $\overline{BL1}$) von dem Schalterkreis (Q15, Q16) wieder miteinander verbunden werden

wobei die aktive Rückstellschaltung (Q5-Q12) in Abhängigkeit von der Aktivierung der Mittel (Q9, Q11) zur Spannungserhöhung eine Bitleitung des einen Bitleitungspaars (BL, $\overline{BL}$, BL1, $\overline{BL1}$) auf eine dritte Spannung auflädt, die größer ist als die erste und die zweite Spannung, wobei dieser Aufladevorgang von den aus der Speicherzelle des Speicherzellen-Arrays (MA) ausgelesenen Daten abhängt.

2. Halbleiterspeicheranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die dritte Spannung gleich Vcc ist.

3. Halbleiterspeicheranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die aktive Rückstellschaltung eine Mehrzahl von Transistoren (Q5-Q12) aufweist und daß die zweite Spannung zu Vcc - Vr gewählt ist, worin Vr eine Schwellenspannung eines der die aktive Rückstellschaltung bildenden Transistoren ist.

FIG. 1 PRIOR ART



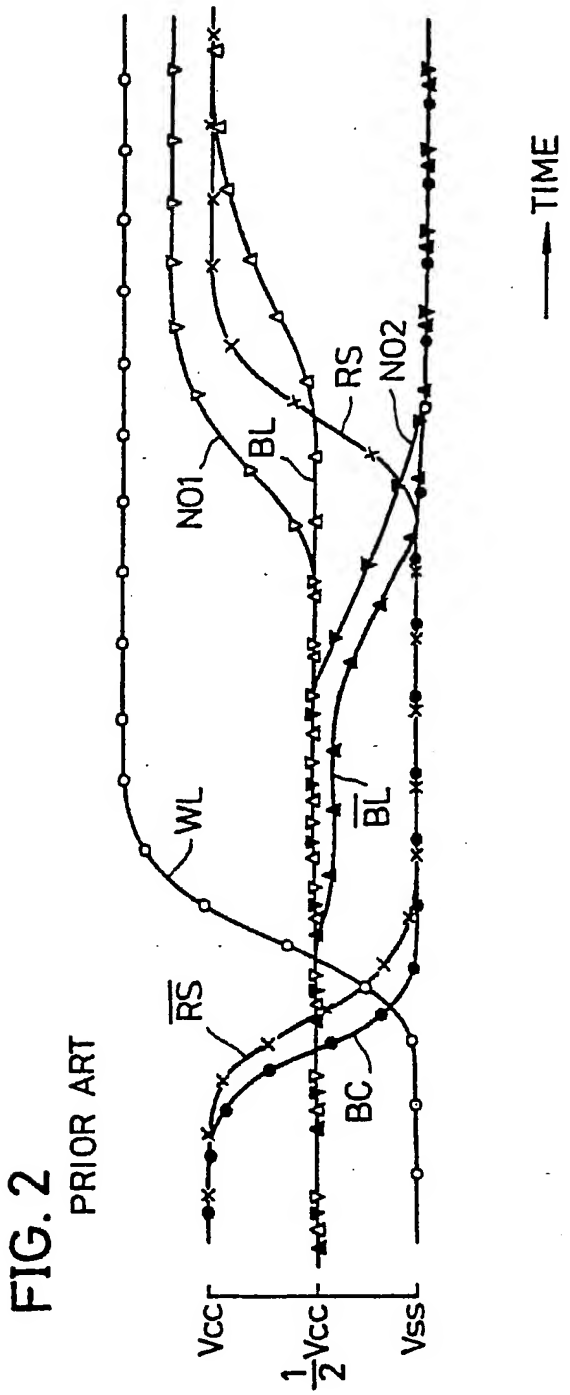
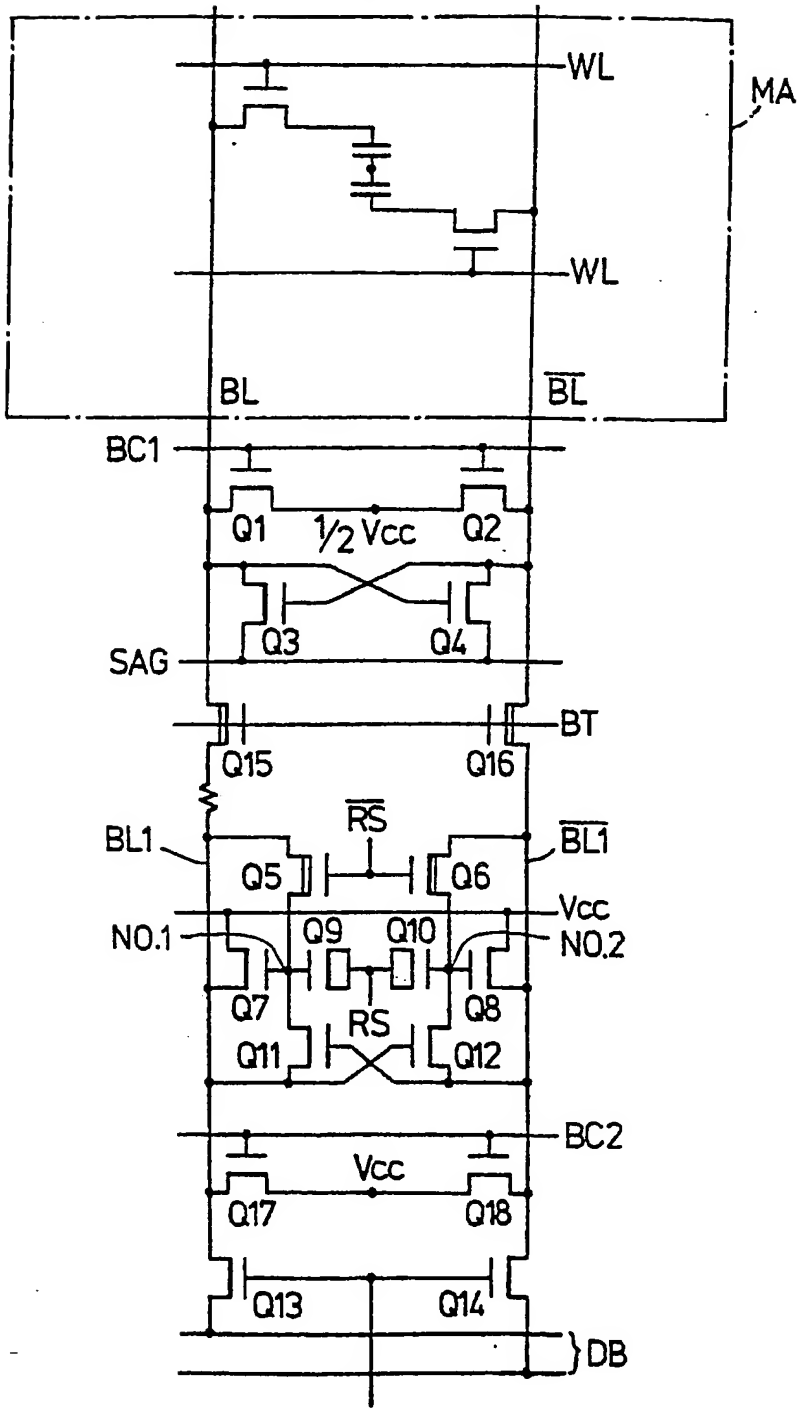


FIG. 2
PRIOR ART

FIG. 3


WL
MA
WL
BL
$\overline{BL}$
BC1
Q1
1/2 Vcc
Q2
Q3
Q4
SAG
BT
Q15
Q16
$\overline{RS}$
BL1
$\overline{BL1}$
Q5
Q6
Vcc
NO.1
Q9
Q10
NO.2
Q7
Q8
RS
Q11
Q12
BC2
Vcc
Q17
Q18
Q13
Q14
DB

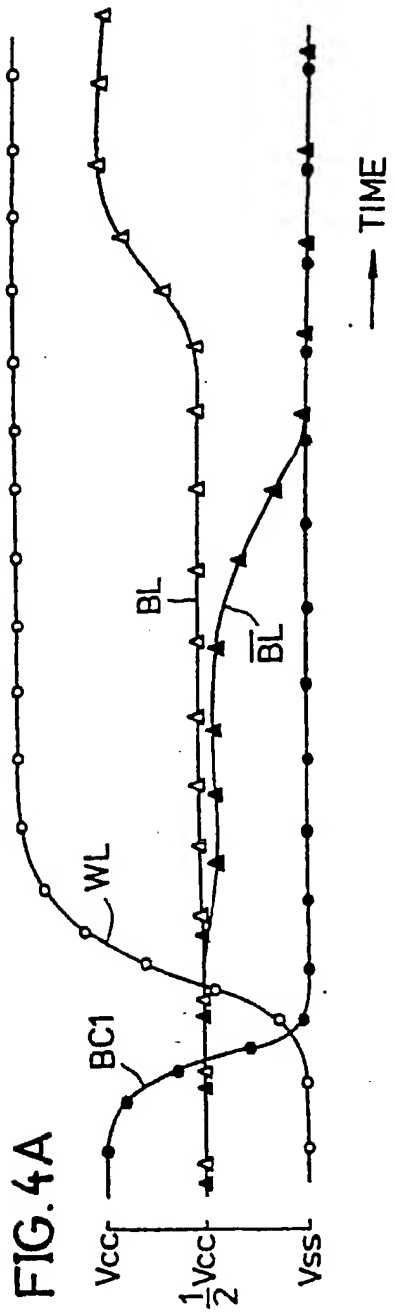

WL
BC1
BL
$\overline{BL}$
Vcc
$\frac{1}{2}$Vcc
Vss
TIME

FIG.4A

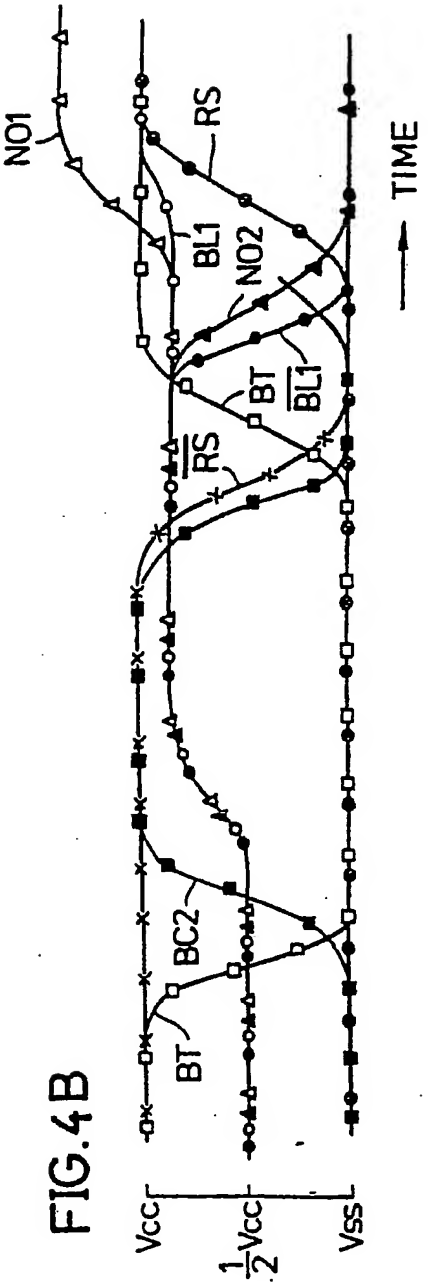

NO1
RS
BL1
NO2
BT
$\overline{BL1}$
$\overline{RS}$
BC2
BT
Vcc
$\frac{1}{2}$Vcc
Vss
TIME

FIG.4B

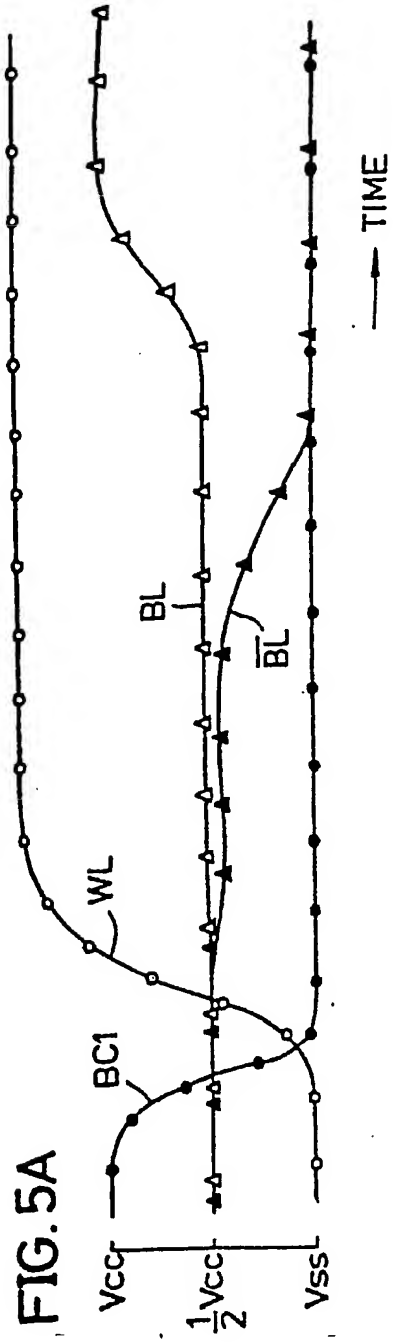

WL
BC1
BL
$\overline{BL}$
Vcc
$\frac{1}{2}$Vcc
Vss
TIME

FIG. 5A

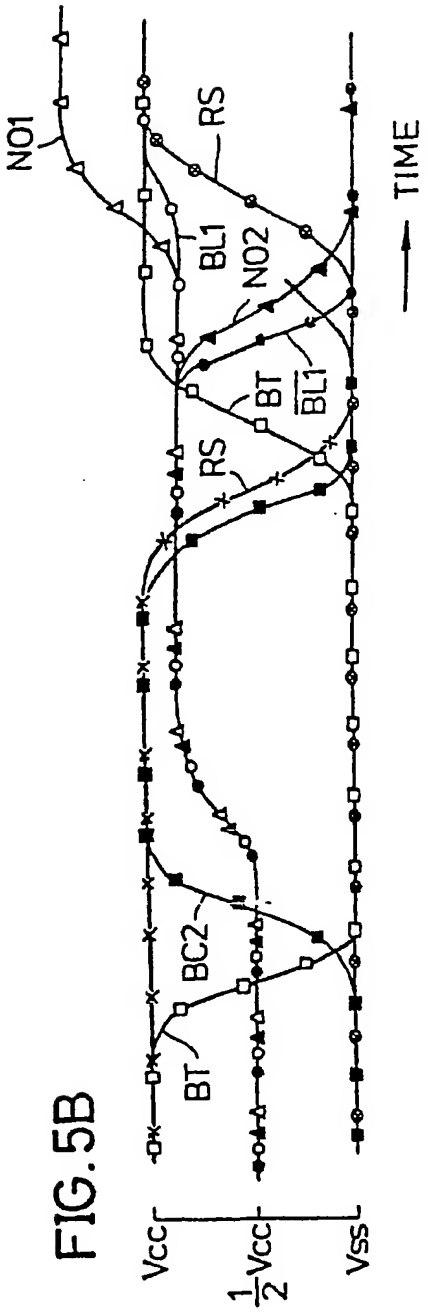

NO1
RS
BL1
NO2
BT
$\overline{BL1}$
RS
BC2
BT
Vcc
$\frac{1}{2}$Vcc
Vss
TIME

FIG. 5B